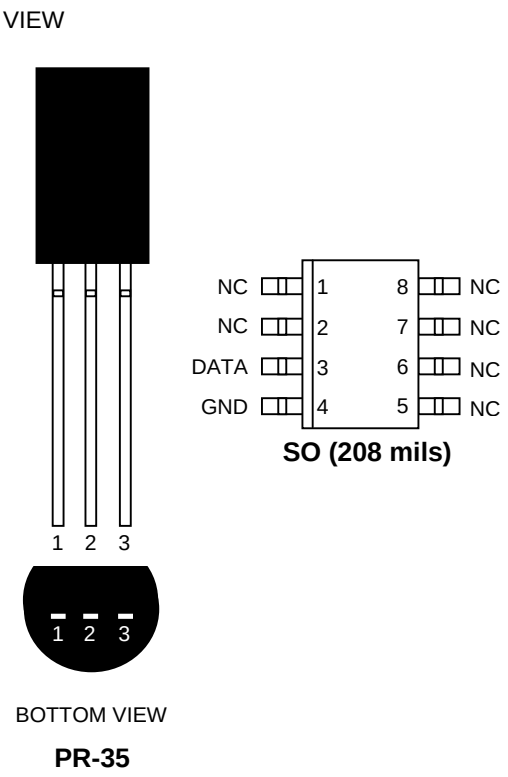
DS2433
4Kb 1-Wire EEPROM

FEATURES

- 4096 Bits Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Unique, Factory-Lasered and Tested 64-Bit Registration Number (8-Bit Family Code + 48-Bit Serial Number + 8-Bit CRC Tester) Assures Absolute Identity Because No Two Parts Are Alike
- Built-In Multidrop Controller Ensures Compatibility with Other MicroLAN Products
- Memory Partitioned Into Sixteen 256-Bit Pages for Packetizing Data
- 256-Bit Scratchpad with Strict Read/Write Protocols Ensures Integrity of Data Transfer
- Reduces Control, Address, Data, and Power to a Single Data Pin
- Directly Connects to a Single Port Pin of a Microprocessor and Communicates at Up to 16.3kbps
- Overdrive Mode Boosts Communication Speed to 142kbps
- 8-Bit Family Code Specifies DS2433 Communication Requirements to Reader
- Presence Detector Acknowledges When Reader First Applies Voltage
- Low-Cost PR-35, SFN, Flip Chip, or 8-Pin SO Surface-Mount Packages
- Reads and Writes Over a Wide Voltage Range of 2.8V to 6.0V from -40°C to +85°C

PIN CONFIGURATIONS



Pin Configurations continued at end of data sheet.

PIN DESCRIPTION

PIN	PR-35	SO	SFN	Flip Chip
1	Ground	NC	Data	Ground
2	Data	NC	Ground	Data
3	NC	Data	—	NC
4	—	Ground	—	NC
5, 6	—	NC	—	NC
7, 8	—	NC	—	—

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2433+	-40°C to +85°C	3 PR-35
DS2433S+	-40°C to +85°C	8 SO
DS2433S+T&R	-40°C to +85°C	8 SO
DS2433G+T&R	-40°C to +85°C	2 SFN
DS2433X#T	-40°C to +85°C	6 Flip Chip (10k pieces)
DS2433X-S#T	-40°C to +85°C	6 Flip Chip (2.5k pieces)

+Denotes a lead-free package.
#Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements.
T/T&R = Tape and reel.

DESCRIPTION

The DS2433 4Kb 1-Wire® EEPROM identifies and stores relevant information about the product to which it is associated. This lot or product specific information can be accessed with minimal interface, for example a single port pin of a microcontroller. The DS2433 consists of a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (23h) plus 4096 bits of user-programmable EEPROM. The power to read and write the DS2433 is derived entirely from the 1-Wire communication line. The memory is organized as sixteen pages of 256 bits each. The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it may be read back for verification. A copy scratchpad command will then transfer the data to memory. This process insures data integrity when modifying the memory. The 64-bit registration number provides a guaranteed unique identity which allows for absolute traceability and acts as node address if multiple DS2433s are connected in parallel to form a local network. Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return. The PR-35 and SO packages provide a compact enclosure that allows standard assembly equipment to handle the device easily for attachment to printed circuit boards or wiring. Typical applications include storage of calibration constants, board identification and product revision status.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2433. The DS2433 has three main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, and 3) 4096-bit EEPROM. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the six ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or 6) Overdrive-Match ROM. Upon completion of an overdrive ROM command byte executed at regular speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 7. All data is read and written least significant bit first.

PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry “steals” power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met.

1-Wire is a registered trademark of Dallas Semiconductor Corp., a wholly owned subsidiary of Maxim Integrated Products, Inc.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground .....-0.5V to +7.0V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP} = 2.8V to 6.0V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1, 8
Logic 0	V_{IL}	-0.3		0.8	V	1, 9
Output Logic-Low at 4mA	V_{OL}			0.4	V	1
Output Logic-High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Programming Current	I_{LPROG}		500		µA	10

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	6

EEPROM

(V_{PUP} = 5.0V, T_A = +25°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write/Erase Cycles	N_{CYCLE}	50k				11

AC ELECTRICAL CHARACTERISTICS—REGULAR SPEED

(V_{PUP} = 2.8V to 6.0V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	13
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	13
Read Data Valid	t_{RDV}		15		µs	12
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	7
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

AC ELECTRICAL CHARACTERISTICS—OVERDRIVE SPEED

(V_{PUP} = 2.8V to 6.0V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	µs	
Write 1 Low Time	t_{LOW1}	1		2	µs	13
Write 0 Low Time	t_{LOW0}	6		16	µs	
Read Low Time	t_{LOWR}	1		2	µs	13
Read Data Valid	t_{RDV}		2		µs	12
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	48			µs	4
Reset Time Low	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDHIGH}	2		6	µs	
Presence Detect Low	t_{PDLOW}	8		24	µs	

NOTES:

1) All voltages are referenced to ground.
2) V_{PUP} = external pullup voltage.
3) Input load is to ground.
4) An additional reset or communication sequence cannot begin until the reset high time has expired.
5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.
6) Capacitance on the data pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to V_{PUP}, 5µs after power has been applied the parasite capacitance will not affect normal communications.
7) The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.
8) V_{IH} is a function of the external pullup resistor and V_{PUP}.
9) Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a Presence Pulse.
10) The Copy Scratchpad takes 5ms maximum during which the voltage on the 1-Wire bus must not fall below 2.8V.
11) During the execution of the Copy Scratchpad command the DS2433 automatically erases the memory locations to be written to. No extra steps need to be taken by the bus master.
12) The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV}. For the case of a read-one time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a read-zero time slot, it ensures that a read will occur before the fastest device(s) release the line.
13) The duration of the low pulse sent by the master should be a minimum of 1µs with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a write-one time or before the master samples in the case of a read-one time.